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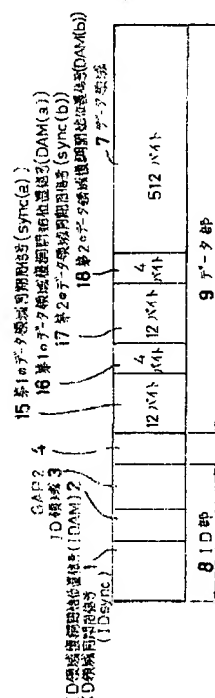
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(54)【発明の名称】 フロッピーディスク装置

(57)【要約】

【目的】 フロッピー・ディスクにおいて、ミッシングパルスやバースト・エラーによる、クロック同期不能や復調開始位置未検出等に起因するセクタエラーの発生率を改善する。

【構成】 セクタフォーマット内にクロック同期用信号 sync 1, 15, 17および復調開始位置信号 DAM 2, 16, 18を、交互にそれぞれ複数個ずつ記録し、いずれか1つのクロック同期用信号 sync によってクロック同期を確立し、その後に位置するいずれか1つの復調開始位置信号 DAMを検出することにより、復調回路を動作させるタイミングを決定する。



【特許請求の範囲】

【請求項1】 セクタ内の再生クロック同期用信号と、再生データ列の復調開始位置を示す復調開始位置信号とを、交互にそれぞれ複数記録した、セクタ単位に情報を記録したフロッピーディスクから、記録された情報を2値化信号に生成する手段と、再生クロック同期信号からフレーム同期信号を生成する手段と、復調開始位置信号を検出して復調開始指示信号を生成する手段と、該復調開始指示信号によって、目的のデータを復調する手段とを備えていることを特徴とするフロッピーディスク装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、コンピュータ等の情報出力装置として使用されるフロッピーディスク装置に関する。

【0002】

【従来の技術】図8は従来のフロッピーディスク(以下、FDと略す)のセクタフォーマットを示している。図8において、1はID領域の信号に再生装置側のクロックを同期させるためのID領域同期用信号(以下、IDsyncと略す)、2はID領域の開始を示すID領域復調開始位置信号(以下、IDAMと略す)、3は各セクタのアドレス情報が記録されているID領域、4はデータ記録再生時にデータ部との緩衝の役目をするGAP、5はデータ領域の信号に再生装置側のクロックを同期させるためのデータ領域同期用信号(以下、syncと略す)、6はデータ領域の開始位置を検出する復調開始位置信号(以下DAMと略す)、7はユーザ情報を記憶するデータ領域である。

【0003】上記セクタフォーマットのIDsync1～ID領域3をID部8、sync5～データ領域7をデータ部9という。

【0004】図9は従来のFD装置の構成を示すブロック図であり、図9において、10はIDsync1およびsync5に装置側のクロックを同期させるクロック同期回路、11はIDAM2およびDAM6を検出する復調開始位置信号検出回路(以下、AM検出回路と略す)、12は同期した信号を復調する復調回路、13は復調されたデータがID部8かデータ部9かを切り分けるスイッチ、14はCPUである。

【0005】次に、上記従来例の動作について説明する。図9において、aは再生信号を2値化した再生パルスであり、クロック同期回路10に入力される。クロック同期回路10は、IDsync1を用いてPLL(Phase Locked Loop)により再生用クロック信号を生成し、この再生クロック信号に同期したパルスデータbを出力する。

【0006】パルスデータbはAM検出回路11及び復調回路12に入力され、AM検出回路11ではIDAM2を検

出してフレーム同期信号cを復調回路12に与え、また、復調回路12ではフレーム同期信号cを受けると復調を開始し、ID領域3の信号をNRZ(Non Return to Zero)信号に復調した復調データdを出力して、スイッチ13に入力する。

【0007】CPU14では、ID部8の再生時にはID領域データhをCPU側に出力するように、ID・データ選択信号gを切り替える。CPU14はこの状態で、ID領域データhを判別し、所望のアドレスでなければ次のセクタを待ち、所望のアドレスであれば続いて記録されているデータ部9のデータ領域再生データeを出力するように、ID・データ選択信号gによってスイッチ13を切り替える。

【0008】その後、上記所望のID検出に続いて、クロック同期回路10はsync5を用いて再生用クロック信号を生成し、パルスデータbを出力する。パルスデータbはAM検出回路11及び復調回路12に入力され、AM検出回路11ではDAM6を検出するとフレーム同期信号cを復調回路12に与える。復調回路12はフレーム同期信号cを受けると復調を開始し、データ領域7の信号をNRZ信号に復調した復調データdを出力し、スイッチ13を通してデータ領域再生データeを出力する。

【0009】以上のように、DAM6はデータの始まりを認識するための重要な信号であり、かつてはDAM6にはDCイレースを使用することが多かったが、最近では、ミッシングパルスなどのデータの欠落を、DAM6として誤検出することがあるために、特定のパターンを使用する方法も増えている。

【0010】

【発明が解決しようとする課題】しかしながら、上記従来のFD装置では、DAM6がデータの欠落(ミッシングパルス)のような欠陥などの理由で検出できない場合に、データ領域の開始位置が検出できず、そのためデータを再生できないことがあった。

【0011】また、sync5に数バイトにおよぶ大きな欠落(以下、バースト・エラーとする)があった場合には、PLLが同期できないため再生用クロック信号が生成できず、したがってDAM6のパターンを検出できなくなり、復調データdが正確に出力されないことがあるという問題点があった。

【0012】すなわち、sync5やDAM6などのデータ領域以外のデータ部9にミッシングパルスやバースト・エラーが発生することによって不良セクタが発生するという問題点があった。

【0013】本発明は、このような従来の問題点を解決することにより、バースト・エラーやミッシングパルスなどにより、DAM6が検出できなかったり、sync5で再生クロック信号が生成できないことに起因する不良セクタの発生率を低下させることのできる優れたFD装置を提供することを目的とするものである。

【0014】

【課題を解決するための手段】本発明は、セクタフォーマット内にsyncおよびDAMを交互にそれぞれ複数個備え、それぞれ、いずれか1つのsyncまたはDAMを検出すれば復調回路を動作させることができるようにしたものである。

【0015】

【作用】本発明によれば、セクタフォーマット内に複数個備えられたDAM、またはsyncのうちいずれか一方を検出すれば良いので、DAMが検出できなかったり、syncで再生用クロック信号が生成できないことに起因する不良セクタの発生率を、著しく低下する。

【0016】

【実施例】図1は本発明の一実施例におけるセクタ・フォーマットを示している。図1において、15は12バイト長の第1のデータ領域同期用信号(以下、sync(a)と略す)、16は4バイト長の第1のデータ領域復調開始位置信号(以下、DAM(a)と略す)、17は12バイト長の第2のデータ領域同期用信号(以下、sync(b)と略す)、18は4バイト長の第2のデータ領域復調開始位置信号(以下、DAM(b)と略す)であり、その他の符号は図8の説明を援用する。

【0017】図2は本発明の第1の実施例のFD装置の構成を示すブロック図である。図2において、10ないし14は図9の対応する部位と同じ、または同機能のもであり、その他の符号で19は遅延回路、20はタイマーである。

【0018】次に、上記本発明における第1の実施例の動作について説明する。aは再生信号を2値化した再生パルスでクロック同期回路10に入力される。クロック同期回路10はIDsync1(図1参照)を用いて再生用クロック信号を生成し、この再生クロック信号に同期したパルスデータbを出力する。

【0019】パルスデータbはAM検出回路11に入力され、1DAM2を検出するとフレーム同期信号cを出力し、遅延回路19に入力する。遅延回路19の遅延量はCPU14からのディレイ指示信号kによって制御され、1D領域3ではその遅延量は0に設定される。

【0020】したがって、遅延回路19から復調回路12にフレーム同期信号c'が出力されるが、1D領域3でのタイミングはAM検出回路11から出力されるフレーム同期信号cに等しい。フレーム同期信号c'を受けた復調回路12では復調を開始し、1D領域3の信号をNRZ信号に復調した復調データdを出力し、スイッチ13に入力する。

【0021】CPU14では、1D部8の再生時にスイッチ13がCPU14に対して1D領域データhを出力するように、1D・データ選択信号gを切り替える。CPU14はこの状態で、1D領域データhを判別し、所望のアドレスでなければ次のセクタを待ち、所望のアドレスであ

れば続いて記録されているデータ部のために、スイッチ13がデータ領域再生データeを出力するように1D・データ選択信号gを切り替える。

【0022】図3は、上記所望の1D領域3を検出した後のデータ部9の再生動作を示すフローチャートである。以下、この図を用いてステップをSと略記して動作を説明する。

【0023】まず、S1では、上述したような手順で所望のデータが記録されているアドレスの1D領域3を検出する。所望の1D領域3を読み出すと続いてS2でクロック同期回路10においてsync(a)15を用いて再生用クロック信号を生成し、S3(a)において、AM検出回路11でDAM(a)16が入力されるのを待ち、何等障害のない場合にはDAM(a)16を検出して、フレーム同期信号cを、遅延回路19、CPU14、およびタイマー20に出力する。

【0024】そしてS5(a)において、遅延回路19はAM検出回路11から受けたフレーム同期信号cを、sync(b)17およびDAM(b)18の分だけ、すなわち16バイト分遅らせて、フレーム同期信号c'を復調回路12に出力する。復調回路12では、このフレーム同期信号c'を受けてデータ領域7の再生パルスを復調し、復調データdとして出力する。

【0025】上記S3(a)でDAM(a)16を検出する際に、S4(a)に示すループで、1D領域3を検出してからDAM(a)16を検出するまでの時間をタイマー20で監視する。

【0026】次に、1D領域3を検出してからDAM(a)16を検出するまでの時間が一定の時間を越えたS4(a)・Yの場合についての、タイムアウト処理についてのべる。1D領域3を検出してからDAM(a)16を検出するまでの時間が、sync(a)15およびDAM(a)16の分を越えた場合、すなわち16バイト分経過してもDAM(a)16が検出できない場合、S3(b)においてDAM(b)18を検出して、フレーム同期信号cを遅延回路19に出力する。

【0027】遅延回路19ではフレーム同期信号cを遅延することなくフレーム同期信号c'を出力する。つまり、sync(a)15で同期を確立し、S5(b)でDAM(a)16とsync(b)17を読み飛ばして、DAM(b)18を検出する。

【0028】DAM(a)16が検出できない原因としては、1つはDAM(a)16そのものの欠陥の場合と、他の1つはsync(a)15で再生用クロック信号が生成できずに検出できない場合とがある。前者の場合は、上記の手順でDAM(b)18を検出するためのデータ領域再生データeは出力されるが、後者の場合は、上記の手順ではDAM(b)18も検出できない。この場合、S7のリトライ・ルーチンによってDAM(b)18を検出することができる。このリトライ・ルーチンの手順を以下、図4によ

て説明する。

【0029】すなわち、図4は、リトライ・ルーチンを示すフローチャートである。S8はS2と同様のID検出手段をあらわしている。S8で所望のID領域3を検出するとsync(a)15およびDAM(a)16の分だけ、すなわち16バイト分遅延させてクロック同期回路10を動作させる。

【0030】次にクロック同期回路10でsync(b)17を用いて再生用クロック信号を生成し、AM検出回路11によってDAM(b)18を検出し、その検出によってフレーム同期信号cを出力する。フレーム同期信号cは、遅延回路19に入力されるが(S9)、ここでは遅延することなくフレーム同期信号c'が出力される(S10)。フレーム同期信号c'は復調回路12に入力され、DAM(b)が検出され(S11)、データ領域7の再生データeが出力される(S13)。また、S11でDAM(b)が検出されないときは、タイムアウト(S12)となり、再生不可能ということになる(S14)。

【0031】したがって、本実施例によると、データ領域復調開始位置信号と同期信号を交互にそれぞれ複数個配置することにより、データ領域復調開始位置信号、あるいは互にそれぞれ複数個配置することにより、データ領域復調開始位置信号DAM(a)、あるいは同期信号sync(a)のバースト・エラーによって不良セクタとなる場合でも、どちらか一方の同期信号で再生用クロック信号を生成し、その後に位置するいずれかのデータ領域復調開始位置信号DAM(b)を検出すれば良いので、データ部8でのエラーに起因する不良セクタの発生率が飛躍的に改善される。

【0032】図5は、本発明の第2の実施例におけるセクタフォーマットを示している。第2の実施例は、第1の実施例のデータ部にエラー訂正用パリティ・バイト35を付加したもので、これはインターリブド・リードソロモンと呼ばれるエラー訂正符号である。

【0033】図6は、図5におけるエラー訂正符号のフォーマットを示す図である。図6のエラー訂正符号の能力はランダム・エラーに対しては3重誤りまで訂正できる。また、バースト・エラーに対しては11バイトの連続したエラーまで訂正することができる。したがって、データ領域およびエラー訂正用パリティ・バイト35については、11バイトまでのバースト・エラーに対して、エラー訂正機能によって正しいデータ領域再生データeを出力することができる。

【0034】図7は本発明の第2の実施例におけるFD装置の構成を示すブロック図であり、36はエラー訂正回路で、その他以下説明したい符号は前図までの符号と同じ、または同等機能のものを指している。

【0035】本発明の第2の実施例の動作は、前述の第1の実施例に示した手順により再生されたデータ領域再生データeにエラーがあった場合に、エラー訂正回路36

によってエラー訂正処理が行われ、データ領域再生データe'として出力される。

【0036】また、syncおよびDAMが記録されている領域に11バイト長までのバースト・エラーがあった場合でも、複数個記録されているsyncおよびDAMのいずれか1つがエラーとなるだけである。したがって、この第2の実施例によると、データ部9のいずれに11バイトまでのバースト・エラーが存在しても、正しいデータ領域再生データe'が出力されることになる。

【0037】ここで、従来のセクタフォーマットに第2の実施例と同じエラー訂正用パリティ・バイト35を付加したと仮定すると、データ領域7およびエラー訂正用パリティ・バイト35にバースト・エラーがあった場合には、そのデータ領域再生データeは正しいものを出力できる。しかし、データ領域7およびエラー訂正用パリティ・バイト35以外にバースト・エラーがあった場合、すなわちsync5やDAM6にバースト・エラーがあった場合には、DAM6が検出できないために復調回路12が動作できず、そのセクタのデータは再生することができなかった。

【0038】したがって、エラー発生要因がデータ部9におけるバースト・エラーである場合、従来のセクタフォーマットではsync5およびDAM6のバースト・エラーが発生するとデータが再生できず、不良セクタとなってしまう可能性が大きい。上記第2の実施例ではsyncおよびDAMのバースト・エラーによる不良セクタの発生率が大きく改善される。

【0039】このように、上記第2の実施例によれば、第1のsync(a)15と第2のsync(b)17のいずれか一方と、その後に位置するDAM(a)16とDAM(b)18のいずれか一方を検出すれば良いことになり、再生用クロック信号を生成できなかったり、DAMが検出できないことに起因する不良セクタの発生率が、大きく改善され、エラー訂正回路18のバースト・エラー訂正能力が十分に利用できるという効果を有する。

【0040】

【発明の効果】以上、説明にしたように本発明のフロッピーディスク装置は、セクタ・フォーマット内にsyncおよびDAMを交互にそれぞれ複数個備え、いずれか1つのsyncで再生用クロック信号を生成し、その後に位置するいずれか1つのDAMを検出することによって、データ領域を再生することができるので、DAMが検出できないことに起因する不良セクタの発生率を著しく低下させることができる。

【0041】また、データ領域にエラー訂正符号に付加したバースト・エラーに対する不良セクタの発生率を低下させた場合に、それぞれのDAMを訂正可能なバースト・エラー長以上離して配置し、その後にsyncを記録しておくことによって、DAMの検出ミスや再生用クロック信号の生成不良に起因する不良セクタの発生率を著

しく低下させることができるために、エラー訂正回路のバースト・エラー訂正能力を十分に利用することができる。

【図面の簡単な説明】

【図1】本発明の第1の実施例におけるセクタフォーマットを示す図である。

【図2】本発明の第1の実施例におけるFD装置の構成を示すブロック図である。

【図3】図2のFD装置の構成を示すフローチャートである。

【図4】図2のFD装置の動作を説明するリトライ・ルーチンのフローチャートである。

【図5】本発明の第2実施例におけるセクタフォーマットを示す図である。

【図6】図5におけるエラー訂正符号フォーマットを示す図である。

【図7】本発明の第2の実施例におけるFD装置の構成

を示すブロック図である。

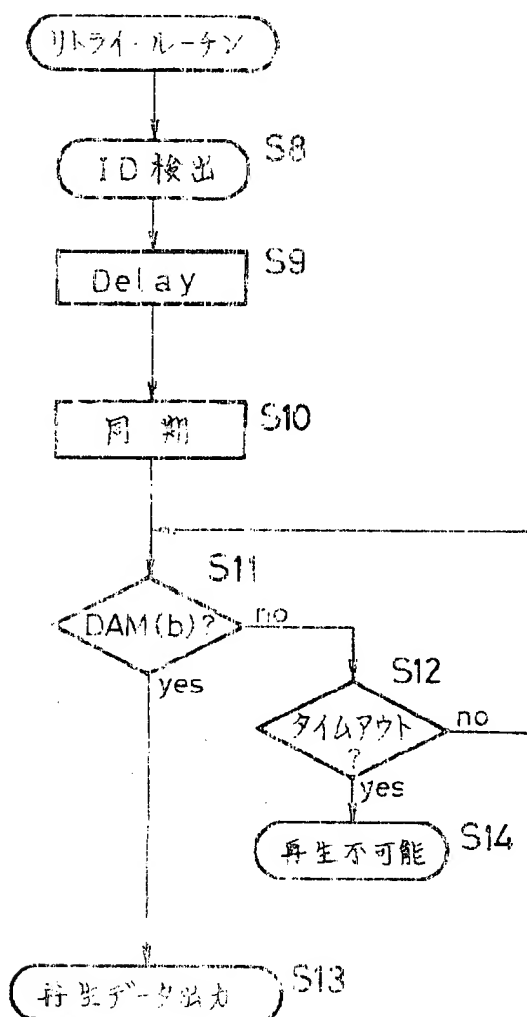
【図8】従来のFD装置のセクタフォーマットを示す図である。

【図9】従来のFD装置の構成を示すブロック図である。

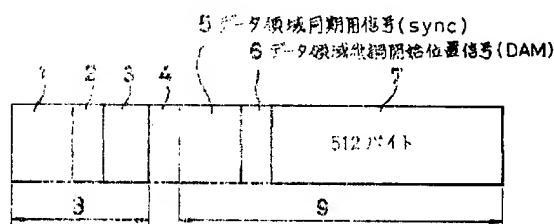
【符号の説明】

1…ID領域同期用信号(IDsync)、2…ID領域復調開始位置信号(IDAM)、3…ID領域、4…GAP2、7…データ領域、8…ID部、9…データ部、10…クロック同期回路、11…復調開始位置信号検出回路(AM検出回路)、12…復調回路、14…CPU、15…第1のデータ領域同期用信号(sync(a))、16…第1のデータ領域復調開始位置信号(DAM(a))、17…第2のデータ領域同期用信号(sync(b))、18…第2のデータ領域復調開始位置信号(DAM(b))、19…遅延回路、20…タイマー、35…エラー訂正用パリティ・バイト、36…エラー訂正回路。

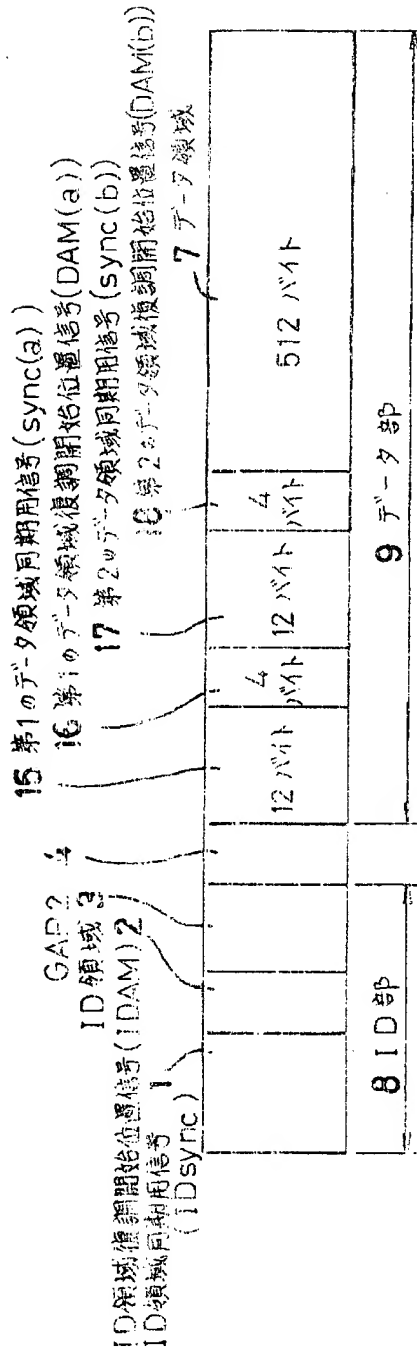
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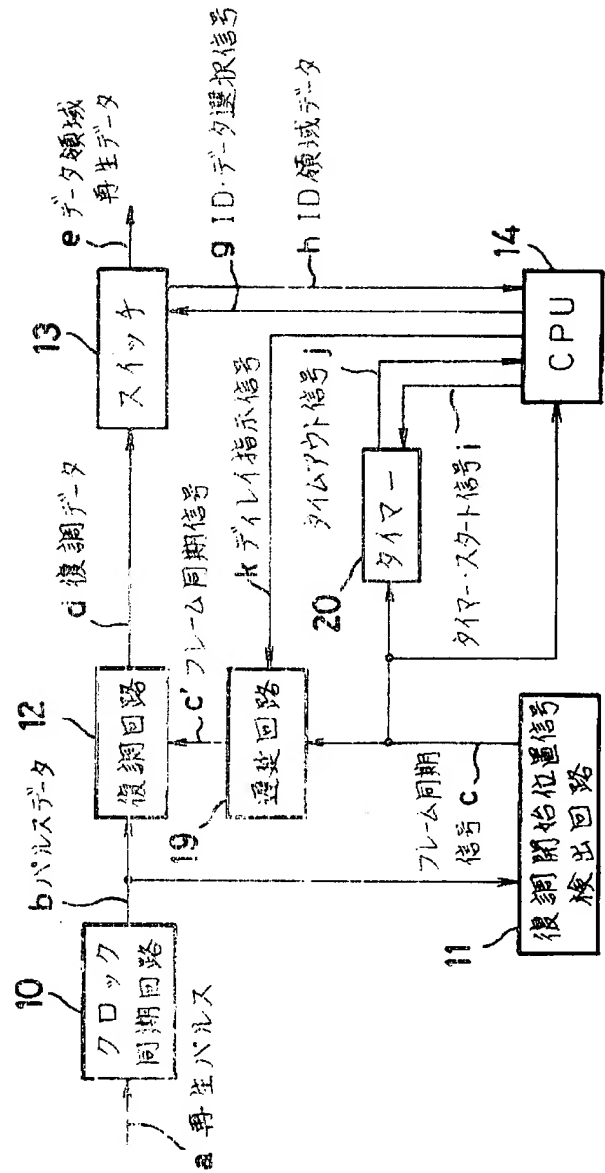
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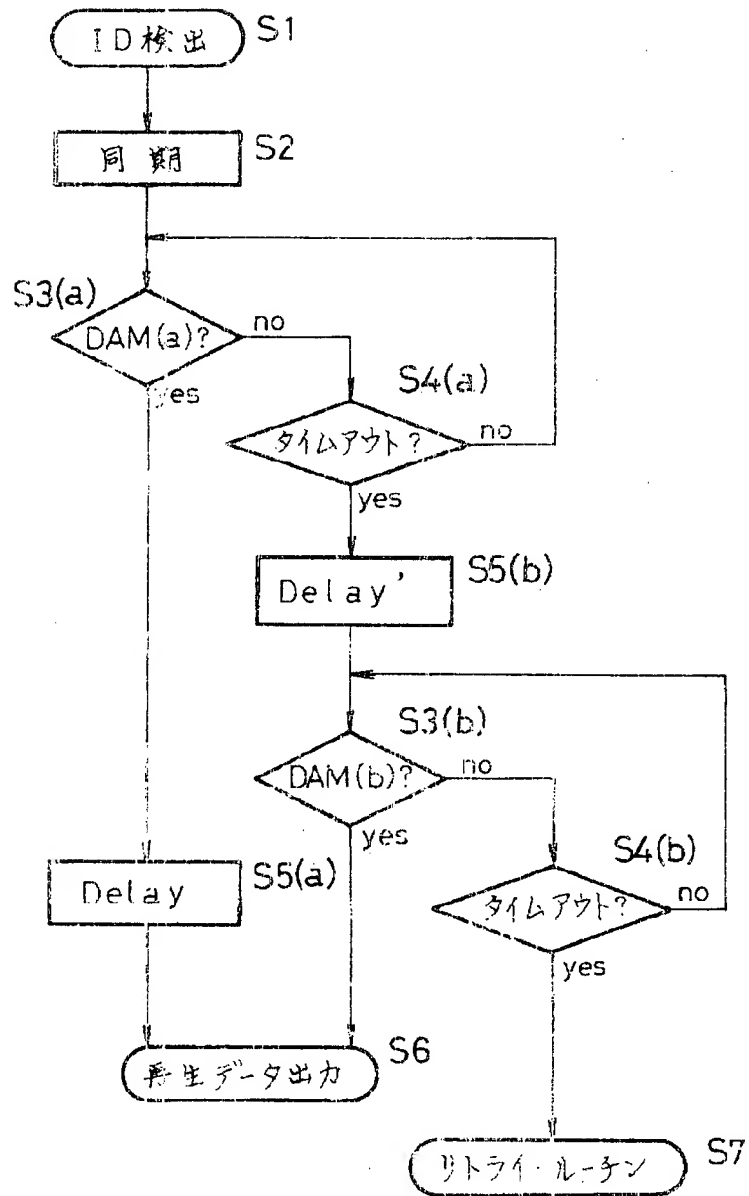
【図1】



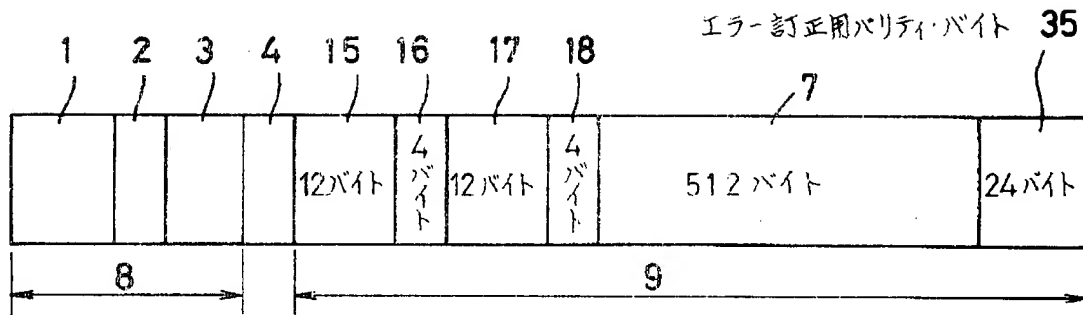
【図2】



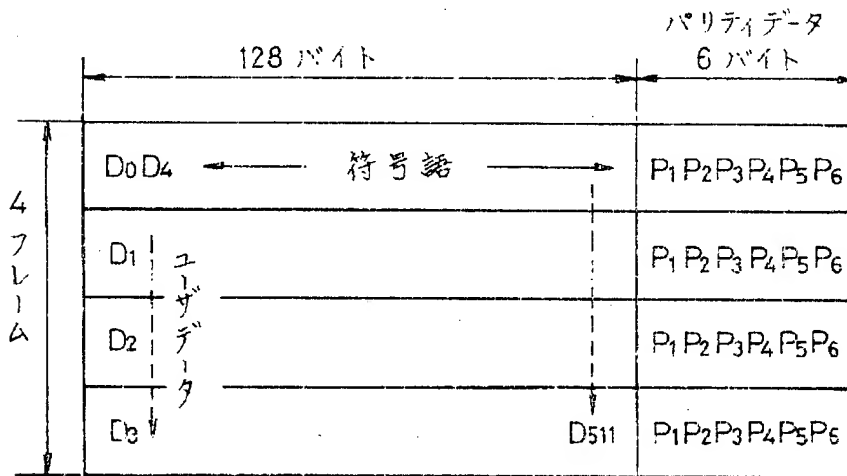
【図3】



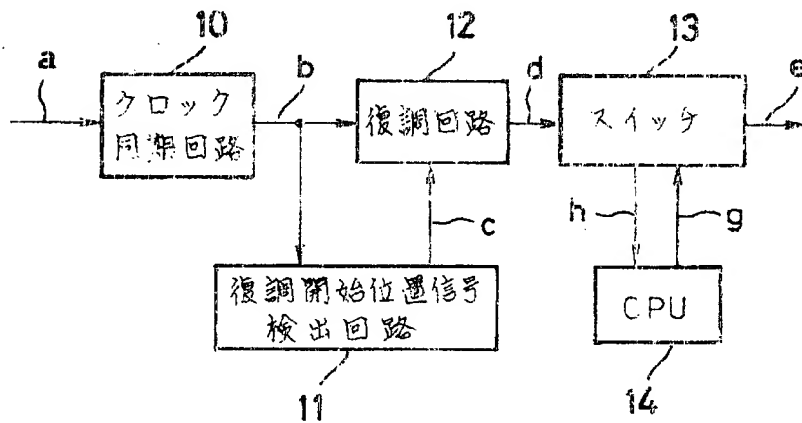
【図5】



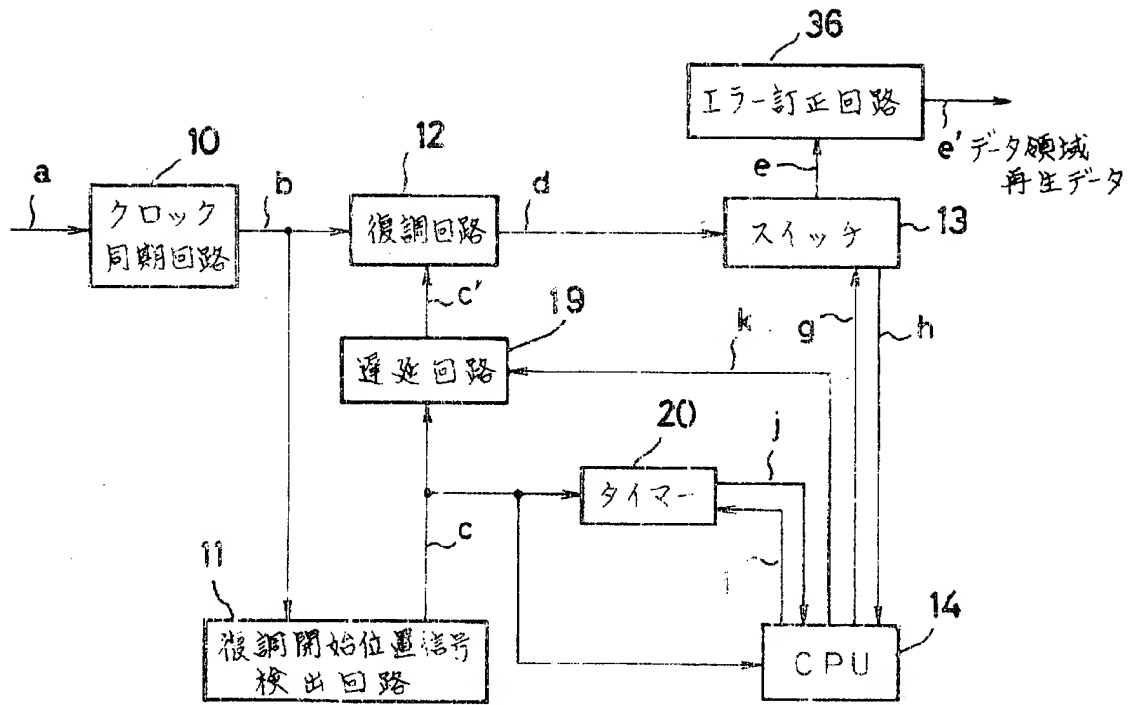
【図6】



【図9】



【図7】





IDEM JOB 0706-101

CERTIFICATION OF ACCURACY

I CERTIFY, UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE UNITED STATES OF AMERICA THAT WE ARE COMPETENT IN **ENGLISH AND JAPANESE** AND THAT THE FOLLOWING ARE, TO THE BEST OF OUR KNOWLEDGE AND BELIEF, A TRUE, CORRECT, COMPLETE AND ACCURATE TRANSLATION OF THE ORIGINAL **DOCUMENTS REGARDING PATENT APPLICATION PUBLIC DISCLOSURE NO H4-26959 AND H5-159465.**

JUNE 21, 2007

A handwritten signature in dark ink, appearing to read 'Mariam Nayiny', is written over a horizontal line.

MARIAM NAYINY
PRESIDENT
IDEM TRANSLATIONS, INC.

Idem Job No. 0706-101 Page 1 of 15
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20/10	351	Z		7923-5D
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Request for examination: Not requested Number of claims: 1 (Total pages: 9)

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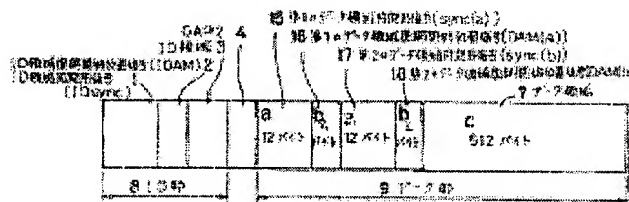
(54) [Title of the Invention]
 Floppy Disk Device

(57) [Abstract]
 [Purpose]

Improves the rate of occurrence of sector errors attributable to the impossibility of clock synchronization, the non-detection of the demodulation start position, etc., as the result of a missing pulse or a burst error, in a floppy disk.

[Constitution]

A plurality of the respective clock synchronization signals sync 1, 15, and 17 and demodulation start position signals DAM 2, 16, and 18 are recorded alternately, multiple respective units at a time, in a sector format; clock synchronization is established by means of any one of the clock synch signals sync; and any one of the demodulation start position signals DAM located thereafter is detected; thus the timing for operating the demodulation circuit is determined.



Key

- 1 1st data area synch signal (IDsync)
- 2 ID area demodulation start position signal (I DAM)
- 3 ID area
- 7 Data area
- 8 ID portion
- 9 Data portion
- 15 1st data area synchronization signal (sync(a))
- 16 1st data area demodulation start position signal (DAM(a))
- 17 2nd data area synchronization signal (sync(b))
- 18 2nd data area demodulation start position signal (DAM(b))
- a 12 bytes
- b 4 bytes
- c 512 bytes

[Claims]

[Claim 1]

A floppy disk device characterized in that [on it] are recorded alternately multiple copies of both a demodulation start position signal that indicates the demodulation start position of the reproduced data string and a reproduction clock synchronization signal within the sector; and [in that it] is equipped with a means of generating the recorded information in a digital signal from a floppy disk on which information is recorded in sector units, a means of generating a frame synchronization signal from the reproduction clock synchronization signal, a means of detecting the demodulation start position signal and generating a demodulation start indication signal, and a means of demodulating the target data by means of the said demodulation start indication signal.

[Detailed Explanation of the Invention]

[0001]

[Field of Industrial Application]

The present invention relates to a floppy disk device used as an information output device, such as a computer.

[0002]

[Prior Art]

The sector format for a conventional floppy disk (hereinafter abbreviated FD) is shown in Figure 8. In Figure 8, 1 is the ID area synchronization signal (hereinafter abbreviated IDsync) for synchronizing the reproduction device-side clock with the ID area signal; 2 is the ID area demodulation start position signal (hereinafter abbreviated IDAM) that indicates the start of the ID area; 3 is the ID area in which the address information for each sector is recorded; 4 is the GAP2 that functions as a buffer with the data portion during data recording and reproduction; 5 is the data area synchronization signal (hereinafter abbreviated sync) for synchronizing the reproduction device-side clock with the data area signal; 6 is the demodulation start position signal (hereinafter abbreviated DAM) that outputs the data area start position; and 7 is the data area in which user information is recorded.

[0003]

The aforementioned sector format's IDsync 1 to ID area 3 is called ID portion 8, and sync 5 to data area 7 is called data portion 9.

[0004]

Figure 9 is a block diagram showing the configuration of a conventional FD device. In Figure 9, 10 is the clock synchronization circuit that synchronizes the device-side clock with IDsync 1 and sync 5. 11 is the demodulation start position signal detection circuit (hereinafter abbreviated AM detection circuit) that detects IDAM 2 and DAM 6; 12 is the demodulation circuit that demodulates the synchronized signal; 13 is the switch that switches between whether the demodulated data is the ID portion 8 or the data portion 9; and 14 is the CPU.

[0005]

Next, the operation of the aforementioned conventional example will be explained. In Figure 9, a is the reproduction pulse that digitizes the reproduced signal, which is input into the clock synchronization circuit 10. The clock synchronization circuit 10 generates the reproduction clock signal by means of a PLL (phase-locked loop) by using IDsync 1, and [it] outputs the pulse data b synchronized with this reproduction clock signal.

[0006]

The pulse data b is input into the AM detection circuit 11 and the demodulation circuit 12, and in the AM detection circuit 11, IDAM 2 is detected and the frame synchronization signal c is provided to the demodulation circuit 12. In addition, when the frame synchronization signal c is received at the demodulation circuit 12, demodulation is started, and the ID area 3 signal is demodulated into an NRZ (non-return-to-zero) signal. The [resulting] demodulated data d is output and input into the switch 13.

[0007]

At the CPU 14, during the reproduction of the ID portion 8, the ID-data selection signal g is switched so as to output to the CPU side the ID area data h. In this state, the CPU 14 determines the ID area data h. If it does not have the desired address, [the CPU] awaits the next sector; if it has the desired address, [the CPU] switches the switch 13 by means of the ID-data selection signal g, so as to output the data area reproduced data e of the recorded data portion 9.

[0008]

Then, after the aforementioned desired ID detection, the clock synchronization circuit 10 generates the clock signal for reproduction, by using sync 5, and outputs the pulse data b. The pulse data b is input into the AM detection circuit 11 and the demodulation circuit 12, and when DAM 6 is detected by the AM detection circuit 11, [it] provides the frame synchronization signal c to the demodulation circuit 12. Upon receiving the frame synchronization signal c, the demodulation circuit 12 outputs the demodulated data d [obtained] by demodulating the signal of the data area 7 into an NRZ signal, [after which it] outputs the data area reproduced data e via the switch 13.

[0009]

As aforementioned, DAM 6 is an important signal for recognizing the start of data. Formerly, DC erase frequently was used for DAM 6. Recently, however, because data loss (e.g., a missing pulse) sometimes is misdetected as DAM 6, an increasing number of methods use a specific pattern.

[0010]

[Problems That the Invention Is to Solve]

However, in the aforementioned conventional FD device, when DAM 6 cannot be detected because of loss, such as data loss (missing pulse), the data area start position cannot be detected, so it sometimes is impossible to reproduce data.

[0011]

Also, when a significant loss (hereinafter, burst error) of several bytes occurs in sync 5, the PLL cannot synchronize, so the clock signal for reproduction cannot be generated. Consequently, a problem results: It becomes impossible to detect the DAM 6 pattern, and the demodulated data d sometimes is not output faithfully.

[0012]

That is, there is a problem in that a bad sector is produced by the occurrence of a missing pulse or burst error in data portion 9 other than data area sync 5, DAM 6, etc.

[0013]

The present invention solves such conventional problems and aims at providing a superior FD device capable of reducing the incidence of bad sectors attributable to the inability to detect DAM 6 and the inability to generate a reproduction clock signal by means of sync 5, as the result of a burst error, missing pulse, etc.

[0014]

[Means of Solving the Problems]

The present invention is [configured] such that it is equipped alternately with multiple sync and DAM in the sector format, and if either sync or DAM is detected, it is possible to operate the demodulation circuit.

[0015]

[Function of the Invention]

According to the present invention, only a DAM or sync, a plurality of which are provided in the sector format, needs to be detected, which significantly reduces the incidence of bad sectors attributable to the inability to detect DAM and the inability to generate a reproduction clock signal by means of sync.

[0016]

[Embodiments]

Figure 1 shows the sector format in one embodiment of the present invention. In Figure 1, 15 is the 12-byte 1st data area synchronization signal (hereinafter abbreviated sync(a)), 16 is the 4-byte 1st data area demodulation start position signal (hereinafter abbreviated DAM(a)), 17 is the 12-byte 2nd data area synchronization signal (hereinafter abbreviated sync(b)), 18 is the 4-byte 2nd data area demodulation start position signal (hereinafter abbreviated DAM(b)), and the other symbols are as explained in Figure 8.

[0017]

Figure 2 is a block diagram showing the configuration of the FD device of the first embodiment of the present invention. In Figure 2, members 10 through 14 correspond to [those in] Figure 9 or have equivalent functionality. As for the other symbols, 19 is the delay circuit, and 20 is the timer.

[0018]

Next, the operation of the aforementioned first embodiment of the present invention will be explained. a is input into the clock synchronization circuit 10 in the reproduction pulse [obtained by] digitizing a reproduction signal. The clock synchronization circuit 10 generates a reproduction clock signal by using IDsync 1 (see Figure 1) and outputs pulse data b synchronized with this reproduction clock signal.

[0019]

The pulse data b is input into the AM detection circuit 11, and when the IDAM 2 is detected, the frame synchronization signal c is output, after which [it] is input into a delay circuit 19. The amount of delay of the delay circuit 19 is controlled by the delay indication signal k from the CPU 14, and the amount of delay is set to 0 in ID area 3.

[0020]

Consequently, the frame synchronization signal c' is output from the delay circuit 19 to the demodulation circuit 12, but the timing in ID area 3 is identical to the frame synchronization signal c output from the AM detection circuit 11. Demodulation starts at the demodulation circuit 12 that received the frame synchronization signal c', and the demodulated data d [obtained by] demodulating the ID area 3 signal to an NRZ signal is output, after which it is input at switch 13.

[0021]

At the CPU 14, the ID-data selection signal g is switched so that, during the reproduction of the ID portion 8, the switch 13 outputs the ID area data h to the CPU 14. In this state, the CPU 14 detects the ID area data h. If [the address] is not the desired address, it awaits the next sector; if it is, it switches the ID-data selection signal g so that the switch 13 outputs the data area reproduced data e, for the continuously recorded data portion.

[0022]

Figure 3 is a flowchart showing the reproduction operation of the data portion 9, after the detection of the aforementioned desired ID area 3. Next, this figure will be used to explain the operation, with "step" abbreviated as S.

[0023]

First, at S1, the ID area 3 of the address, in which is recorded the desired data, is detected by means of the aforementioned procedure. At S2, after the desired ID area 3 is read, the reproduction clock signal is generated by using sync(a)¹ 15 in the clock synchronization circuit 10. At S3(a), [execution] waits until DAM(a) 16 is input by the AM detection circuit 11. If there is no problem, DAM(a) 16 is detected and the frame synchronization signal c is output to the delay circuit 19, the CPU 14, and the timer 20.

¹ Translator's note: The Japanese patent contains the typo "syne(a)."

[0024]

Then, at S5(a), the delay circuit 19 delays the frame synchronization signal c received from the AM detection circuit 11, by the amount of sync(b) 17 and DAM(b) 18 (i.e., by 16 bytes) and outputs the frame synchronization c' to the demodulation circuit 12. At the demodulation circuit 12, this frame synchronization c' is received, and the reproduction pulse for the data area 7 is demodulated and output as the demodulated data d.

[0025]

When DAM(a) 16 is detected at the aforementioned S3(a), the loop S4(a) is used to monitor with the timer 20 the time from the detection of the ID area 3 to the detection of DAM(a) 16.

[0026]

Next explained will be the timeout process for the Y case at S4(a), where the time from the detection of the ID area 3 to the detection of the DAM(a) 16 exceeds a given time period. If DAM(a) 16 is not detected even after the time from the detection of the ID area 3 to the detection of DAM(a) 16 exceeds the amounts of sync(a) 15 and DAM(a) 16 (i.e., after the passage of 16 bytes), at S3(b) DAM(b) 18 is detected and the frame synchronization signal c is output to the delay circuit 19.

[0027]

At the delay circuit 19, the frame synchronization signal c' is output without delaying the frame synchronization signal c. That is, synchronization is established by sync(a) 15, and at S5(b) DAM(a) 16 and sync(b) 17 are skipped and DAM(b) 18 is detected.

[0028]

The two causes of the non-detection of DAM(a) 16 are, first, a defective DAM(a) 16 itself and, second, the inability to detect the reproduction block signal because it was not generated by sync(a) 15. In the former case, the data area reproduced data e for detecting DAM(b) 18 by means of the aforementioned procedure is output; however, in the latter case, DAM(b) 18 also is undetectable by means of the aforementioned procedure. In this case, it is possible to detect DAM(b) 18 by means of the retry routine at S7. Next, this retry routine procedure will be explained with reference to Figure 4.

[0029]

That is, Figure 4 is a flowchart showing the retry routine. S8 indicates an ID detection means identical to [that of] S2. At S8, when the desired ID area 3 is detected, the clock synchronization circuit 10 is operated after a delay in the amount of sync(a) 15 and DAM(a) 16 (i.e., 16 bytes).

[0030]

Next, at the clock synchronization circuit 10, sync(b) 17 is used to generate the playback clock signal, the AM detection circuit 11 detects DAM(b) 18, and the frame synchronization signal c is output as the result of this detection. The frame synchronization signal c is input into the delay circuit 19 (S9). Here, however, the frame

synchronization signal c' is output without a delay (S10). The frame synchronization signal c' is input into the demodulation circuit 12, DAM(b) is output (S11), and the reproduced data e of data area 7 is output (S13). Also, at S11, if DAM(b) is not detected, a timeout (S12) results, so reproduction becomes impossible (S14).

[0031]

Consequently, according to the present embodiment, by alternately disposing multiple data area demodulation start position signals and synchronization signals, and by disposing the data area demodulation start position signal or multiple [copies] thereof, even if a bad sector results from a burst error of synchronization signal sync(a) or data area demodulation start position signal (DAM)(a), either of the data area demodulation start positions signals DAM(b) located thereafter may be detected, thereby dramatically improving the incidence of bad sectors attributable to error, in data portion 8.

[0032]

The sector format in the second embodiment of the present invention is shown in Figure 5. In the second embodiment, error-correction parity bytes 35 are added to the data portion of the first embodiment, and this is an error-correction code called interleaved Reed-Solomon.

[0033]

Figure 6 is a diagram showing the format of the error-correction code in Figure 5. The performance of the error-correction code of Figure 6 enables triple error [correction] of random errors. Also, for burst errors, it is possible to correct up to 11 continuous bytes of errors. Consequently, for the data area and error-correction parity bytes 35, it is possible to output the correct data area reproduced data e by means of the error-correction function, for burst errors up to 11 bytes.

[0034]

Figure 7 is the block diagram showing the configuration of the FD device of the second embodiment of the present invention. 36 is the error-correction circuit, and other symbols not explained hereinafter indicate functionalities identical or equivalent to those of symbols in previous diagrams.

[0035]

Regarding the operation of the second embodiment of the present invention, when an error occurs in the data area reproduced data e reproduced by means of the procedure in the first embodiment of the present invention, error-correction processing is performed by the error-correction circuit 36, and [the result] is output as the data area reproduced data e' .

[0036]

In addition, even if a burst error up to 11 bytes long occurs in the area in which sync and DAM are recorded, only one of the multiple recorded syncs [or] DAMs will become an error. Consequently, according to this second embodiment, even if a burst error up to 11 bytes is present anywhere in data portion 9, the correct data area reproduced data e' will be output.

[0037]

Here, supposing that the same error-correction parity bytes 35 as [those] in the second embodiment are added to the conventional sector format, when a burst error occurs in the data area 7 and the error-correction parity bytes 35, the correct data area reproduced data e can be output. However, when a burst error occurs elsewhere than in data area 7 [or] the error-correction parity bytes 35 (i.e., when a burst error occurs in sync 5 or DAM 6), DAM 6 cannot be detected, so the demodulation circuit 12 cannot operate and the center data cannot be reproduced.

[0038]

Consequently, when an error is caused by a burst error in the data portion 9, if a sync 5 and DAM 6 burst error occurs in the conventional sector format, the data cannot be reproduced, and it is highly probable that a bad sector will result. In the aforementioned second embodiment, however, the incidence of bad sectors resulting from sync and DAM burst errors is improved considerably.

[0039]

Thus, the aforementioned second embodiment has [the following] effects: It is only necessary to detect either the first sync(a) 15 [or] the second sync(b) 17 as well as either DAM(a) 16 [or] DAM(b) 18 located thereafter, so there is considerable improvement in the incidence of bad sectors attributable to the inability to generate the clock signal for reproduction and the inability to detect DAM, and the burst error-correction capability of the error-correction circuit 18 can be utilized well.

[0040]

[Effects of the Invention]

The floppy disk device of the present invention, which was explained previously, is equipped with multiple, alternate sync and DAM in the sector format, and [it] can considerably reduce the incidence of bad sectors attributable to the inability to detect DAM, because it is possible to reproduce the data area by generating a reproduction clock signal by means of either sync and detecting either DAM located thereafter.

[0041]

In addition, when an error-correction code is added to the data area to reduce the incidence of bad sectors attributable to bad sectors, each DAM is disposed at least the correctable burst error length apart, and sync is recorded thereafter. As a result, it is possible to significantly reduce the incidence of bad sectors attributable to DAM detection mistakes and reproduction clock signal generation trouble. Therefore, it is possible to make good use of the burst error-correction capability of the error-correction circuit.

[Brief Explanation of the Drawings]

[Figure 1]

A diagram showing the sector format in the first embodiment of the present invention.

[Figure 2]

A block diagram showing the configuration of the FD device in the first embodiment of the present invention.

[Figure 3]

A flowchart showing the configuration of the FD device of Figure 2.

[Figure 4]

The retry routine flowchart that explains the operation of the FD device of Figure 2.

[Figure 5]

A diagram showing the sector format in the second embodiment of the present invention.

[Figure 6]

A diagram showing the error-correction code format in Figure 5.

[Figure 7]

A block diagram showing the configuration of the FD device in the second embodiment of the present invention.

[Figure 8]

A diagram showing the sector format of a conventional FD device.

[Figure 9]

A block diagram showing the configuration of a conventional FD device.

[Explanation of the Symbols]

- 1 ID area synchronization signal (IDsync)
- 2 ID area demodulation start position signal (IDAM)
- 3 ID area
- 4 GAP2
- 7 Data area
- 8 ID portion
- 9 Data portion
- 10 Clock synchronization circuit
- 11 Demodulation start position signal detection circuit (AM detection circuit)
- 12 Demodulation circuit
- 14 CPU
- 15 1st data area synchronization signal (sync(a))
- 16 1st data area demodulation start position signal (DAM(a))
- 17 2nd data area synchronization signal (sync(b))
- 18 2nd data area demodulation start position signal (DAM(b))
- 19 Delay circuit
- 20 Timer
- 35 Error-correction parity bytes
- 36 Error-correction circuit

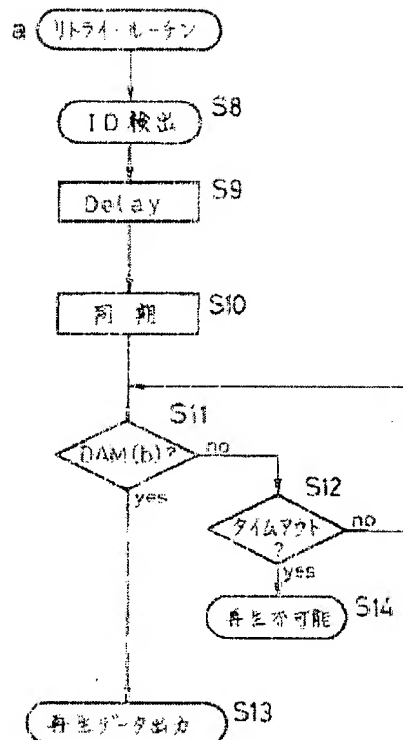


Figure 4

Key
 a Retry routine
 S8 ID detection
 S10 Synchronization
 S12 Timeout?
 S13 Reproduced data output
 S14 Reproduction impossible

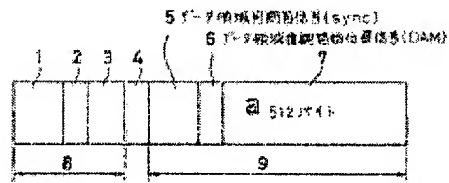


Figure 8

Key
 5 Data area synchronization signal (sync)
 6 Data area demodulation start position signal (DAM)
 a 512 bytes

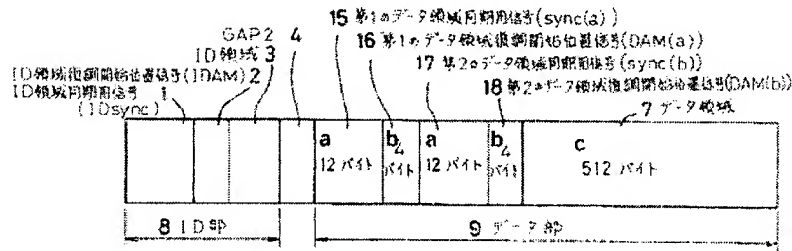


Figure 1

Key

- 1 ID area synchronization signal (IDsync)
- 2 ID area demodulation start position signal (IDAM)
- 3 ID area
- 7 Data area
- 8 ID portion
- 9 Data portion
- 15 1st data area synchronization signal (sync(a))
- 16 1st data area demodulation start position signal (DAM(a))
- 17 2nd data area synchronization signal (sync(b))
- 18 2nd data area demodulation start position signal (DAM(b))
- a 12 bytes
- b 4 bytes
- c 512 bytes

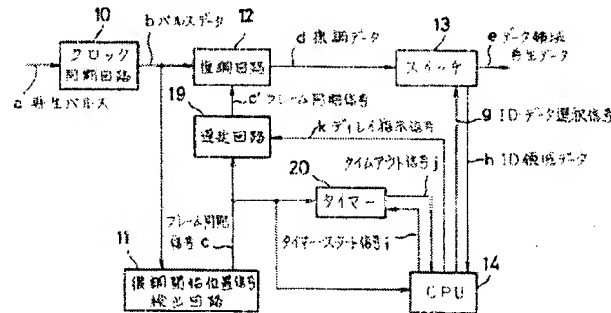


Figure 2

Key

- 10 Clock sync circuit
- 11 Demodulation start position signal detection circuit
- 12 Demodulation circuit
- 13 Switch
- 19 Delay circuit
- 20 Timer
- a Reproduction pulse
- b Pulse data
- c Frame synchronization signal
- c' Frame synchronization signal
- d Demodulated data
- e Data area reproduced data
- g ID-data select signal
- h ID area data
- i Timer start signal
- j Timeout signal
- k Delay indication signal

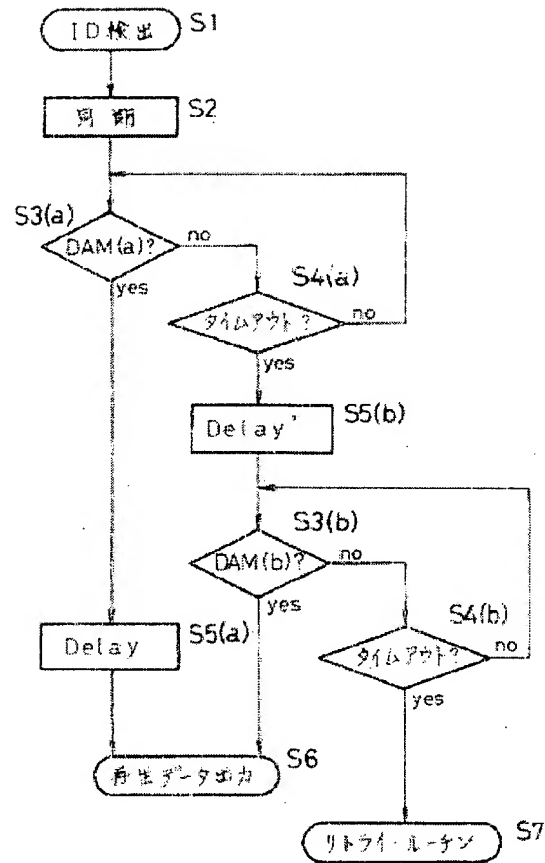


Figure 3

Key

- S1 ID detection
- S2 Synchronization
- S4(a) Timeout?
- S4(b) Timeout?
- S6 Reproduced data output
- S7 Retry routine

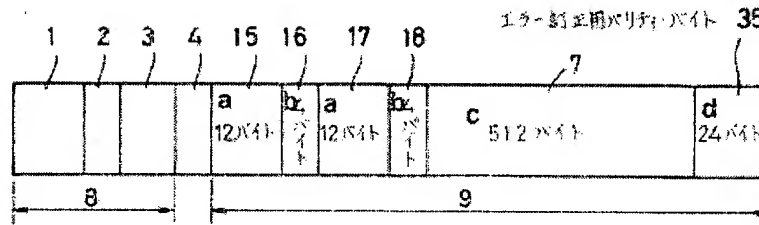


Figure 5

Key
 7 512 bytes
 a 12 bytes
 b 4 bytes
 c 512 bytes
 d 24 bytes

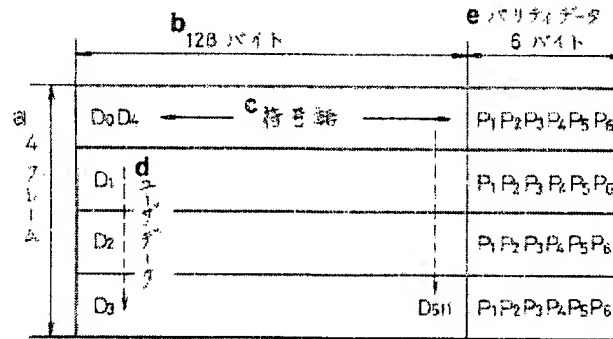


Figure 6

Key
 a 4 frames
 b 128 bytes
 c Code words
 d User data
 e Parity data, 6 bytes

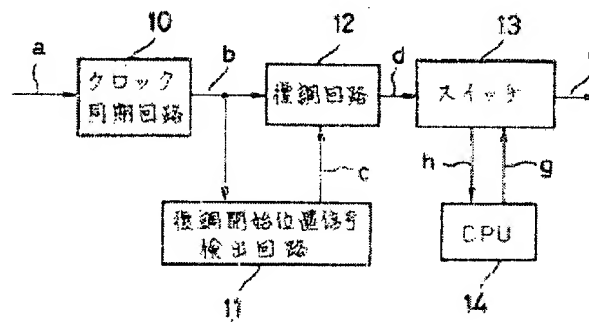


Figure 9

Key
 10 Clock sync circuit
 11 Demodulation start position signal detection circuit
 12 Demodulation circuit
 13 Switch

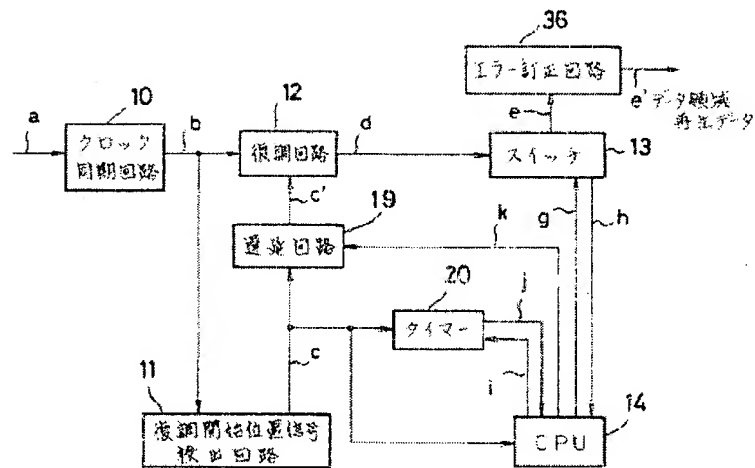


Figure 7

Key

- 10 Clock sync circuit
- 11 Demodulation start position signal detection circuit
- 12 Demodulation circuit
- 13 Switch
- 19 Delay circuit
- 20 Timer
- 36 Error-correction circuit
- e' Data area reproduced data

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20/14	351	A		8322-5D

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(54) [Title of the Invention]

Floppy Disk Device

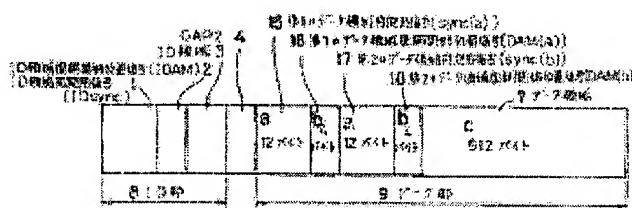
(57) [Abstract]

[Purpose]

Improves the rate of occurrence of sector errors attributable to the impossibility of clock synchronization, the non-detection of the demodulation start position, etc., as the result of a missing pulse or a burst error, in a floppy disk.

[Constitution]

A plurality of the respective clock synchronization signals sync 1, 15, and 17 and demodulation start position signals DAM 2, 16, and 18 are recorded alternately, multiple respective units at a time, in a sector format; clock synchronization is established by means of any one of the clock synch signals sync; and any one of the demodulation start position signals DAM located thereafter is detected; thus the timing for operating the demodulation circuit is determined.



Key

- 1 1st data area sync signal (IDsync)
- 2 ID area demodulation start position signal (I DAM)
- 3 ID area
- 7 Data area
- 8 ID portion
- 9 Data portion
- 15 1st data area synchronization signal (sync(a))
- 16 1st data area demodulation start position signal (DAM (a))
- 17 2nd data area synchronization signal (sync(b))
- 18 2nd data area demodulation start position signal (DAM(b))
- a 12 bytes
- b 4 bytes
- c 512 bytes

[Claims]

[Claim 1]

A floppy disk device characterized in that [on it] are recorded alternately multiple copies of both a demodulation start position signal that indicates the demodulation start position of the reproduced data string and a reproduction clock synchronization signal within the sector; and [in that it] is equipped with a means of generating the recorded information in a digital signal from a floppy disk on which information is recorded in sector units, a means of generating a frame synchronization signal from the reproduction clock synchronization signal, a means of detecting the demodulation start position signal and generating a demodulation start indication signal, and a means of demodulating the target data by means of the said demodulation start indication signal.

[Detailed Explanation of the Invention]

[0001]

[Field of Industrial Application]

The present invention relates to a floppy disk device used as an information output device, such as a computer.

[0002]

[Prior Art]

The sector format for a conventional floppy disk (hereinafter abbreviated FD) is shown in Figure 8. In Figure 8, 1 is the ID area synchronization signal (hereinafter abbreviated IDsync) for synchronizing the reproduction device-side clock with the ID area signal; 2 is the ID area demodulation start position signal (hereinafter abbreviated IDAM) that indicates the start of the ID area; 3 is the ID area in which the address information for each sector is recorded; 4 is the GAP2 that functions as a buffer with the data portion during data recording and reproduction; 5 is the data area synchronization signal (hereinafter abbreviated sync) for synchronizing the reproduction device-side clock with the data area signal; 6 is the demodulation start position signal (hereinafter abbreviated DAM) that outputs the data area start position; and 7 is the data area in which user information is recorded.

[0003]

The aforementioned sector format's IDsync 1 to ID area 3 is called ID portion 8, and sync 5 to data area 7 is called data portion 9.

[0004]

Figure 9 is a block diagram showing the configuration of a conventional FD device. In Figure 9, 10 is the clock synchronization circuit that synchronizes the device-side clock with IDsync 1 and sync 5. 11 is the demodulation start position signal detection circuit (hereinafter abbreviated AM detection circuit) that detects IDAM 2 and DAM 6; 12 is the demodulation circuit that demodulates the synchronized signal; 13 is the switch that switches between whether the demodulated data is the ID portion 8 or the data portion 9; and 14 is the CPU.

[0005]

Next, the operation of the aforementioned conventional example will be explained. In Figure 9, a is the reproduction pulse that digitizes the reproduced signal, which is input into the clock synchronization circuit 10. The clock synchronization circuit 10 generates the reproduction clock signal by means of a PLL (phase-locked loop) by using IDsync 1, and [it] outputs the pulse data b synchronized with this reproduction clock signal.

[0006]

The pulse data b is input into the AM detection circuit 11 and the demodulation circuit 12, and in the AM detection circuit 11, IDAM 2 is detected and the frame synchronization signal c is provided to the demodulation circuit 12. In addition, when the frame synchronization signal c is received at the demodulation circuit 12, demodulation is started, and the ID area 3 signal is demodulated into an NRZ (non-return-to-zero) signal. The [resulting] demodulated data d is output and input into the switch 13.

[0007]

At the CPU 14, during the reproduction of the ID portion 8, the ID-data selection signal g is switched so as to output to the CPU side the ID area data h. In this state, the CPU 14 determines the ID area data h. If it does not have the desired address, [the CPU] awaits the next sector; if it has the desired address, [the CPU] switches the switch 13 by means of the ID-data selection signal g, so as to output the data area reproduced data e of the recorded data portion 9.

[0008]

Then, after the aforementioned desired ID detection, the clock synchronization circuit 10 generates the clock signal for reproduction, by using sync 5, and outputs the pulse data b. The pulse data b is input into the AM detection circuit 11 and the demodulation circuit 12, and when DAM 6 is detected by the AM detection circuit 11, [it] provides the frame synchronization signal c to the demodulation circuit 12. Upon receiving the frame synchronization signal c, the demodulation circuit 12 outputs the demodulated data d [obtained] by demodulating the signal of the data area 7 into an NRZ signal, [after which it] outputs the data area reproduced data e via the switch 13.

[0009]

As aforementioned, DAM 6 is an important signal for recognizing the start of data. Formerly, DC erase frequently was used for DAM 6. Recently, however, because data loss (e.g., a missing pulse) sometimes is misdetected as DAM 6, an increasing number of methods use a specific pattern.

[0010]

[Problems That the Invention Is to Solve]

However, in the aforementioned conventional FD device, when DAM 6 cannot be detected because of loss, such as data loss (missing pulse), the data area start position cannot be detected, so it sometimes is impossible to reproduce data.

[0011]

Also, when a significant loss (hereinafter, burst error) of several bytes occurs in sync 5, the PLL cannot synchronize, so the clock signal for reproduction cannot be generated. Consequently, a problem results: It becomes impossible to detect the DAM 6 pattern, and the demodulated data d sometimes is not output faithfully.

[0012]

That is, there is a problem in that a bad sector is produced by the occurrence of a missing pulse or burst error in data portion 9 other than data area sync 5, DAM 6, etc.

[0013]

The present invention solves such conventional problems and aims at providing a superior FD device capable of reducing the incidence of bad sectors attributable to the inability to detect DAM 6 and the inability to generate a reproduction clock signal by means of sync 5, as the result of a burst error, missing pulse, etc.

[0014]

[Means of Solving the Problems]

The present invention is [configured] such that it is equipped alternately with multiple sync and DAM in the sector format, and if either sync or DAM is detected, it is possible to operate the demodulation circuit.

[0015]

[Function of the Invention]

According to the present invention, only a DAM or sync, a plurality of which are provided in the sector format, needs to be detected, which significantly reduces the incidence of bad sectors attributable to the inability to detect DAM and the inability to generate a reproduction clock signal by means of sync.

[0016]

[Embodiments]

Figure 1 shows the sector format in one embodiment of the present invention. In Figure 1, 15 is the 12-byte 1st data area synchronization signal (hereinafter abbreviated sync(a)), 16 is the 4-byte 1st data area demodulation start position signal (hereinafter abbreviated DAM(a)), 17 is the 12-byte 2nd data area synchronization signal (hereinafter abbreviated sync(b)), 18 is the 4-byte 2nd data area demodulation start position signal (hereinafter abbreviated DAM(b)), and the other symbols are as explained in Figure 8.

[0017]

Figure 2 is a block diagram showing the configuration of the FD device of the first embodiment of the present invention. In Figure 2, members 10 through 14 correspond to [those in] Figure 9 or have equivalent functionality. As for the other symbols, 19 is the delay circuit, and 20 is the timer.

[0018]

Next, the operation of the aforementioned first embodiment of the present invention will be explained. a is input into the clock synchronization circuit 10 in the reproduction pulse [obtained by] digitizing a reproduction signal. The clock synchronization circuit 10 generates a reproduction clock signal by using IDsync 1 (see Figure 1) and outputs pulse data b synchronized with this reproduction clock signal.

[0019]

The pulse data b is input into the AM detection circuit 11, and when the IDAM 2 is detected, the frame synchronization signal c is output, after which [it] is input into a delay circuit 19. The amount of delay of the delay circuit 19 is controlled by the delay indication signal k from the CPU 14, and the amount of delay is set to 0 in ID area 3.

[0020]

Consequently, the frame synchronization signal c' is output from the delay circuit 19 to the demodulation circuit 12, but the timing in ID area 3 is identical to the frame synchronization signal c output from the AM detection circuit 11. Demodulation starts at the demodulation circuit 12 that received the frame synchronization signal c', and the demodulated data d [obtained by] demodulating the ID area 3 signal to an NRZ signal is output, after which it is input at switch 13.

[0021]

At the CPU 14, the ID-data selection signal g is switched so that, during the reproduction of the ID portion 8, the switch 13 outputs the ID area data h to the CPU 14. In this state, the CPU 14 detects the ID area data h. If [the address] is not the desired address, it awaits the next sector; if it is, it switches the ID-data selection signal g so that the switch 13 outputs the data area reproduced data e, for the continuously recorded data portion.

[0022]

Figure 3 is a flowchart showing the reproduction operation of the data portion 9, after the detection of the aforementioned desired ID area 3. Next, this figure will be used to explain the operation, with "step" abbreviated as S.

[0023]

First, at S1, the ID area 3 of the address, in which is recorded the desired data, is detected by means of the aforementioned procedure. At S2, after the desired ID area 3 is read, the reproduction clock signal is generated by using sync(a)¹ 15 in the clock synchronization circuit 10. At S3(a), [execution] waits until DAM(a) 16 is input by the AM detection circuit 11. If there is no problem, DAM(a) 16 is detected and the frame synchronization signal c is output to the delay circuit 19, the CPU 14, and the timer 20.

¹ Translator's note: The Japanese patent contains the typo "syne(a)."

[0024]

Then, at S5(a), the delay circuit 19 delays the frame synchronization signal c received from the AM detection circuit 11, by the amount of sync(b) 17 and DAM(b) 18 (i.e., by 16 bytes) and outputs the frame synchronization c' to the demodulation circuit 12. At the demodulation circuit 12, this frame synchronization c' is received, and the reproduction pulse for the data area 7 is demodulated and output as the demodulated data d.

[0025]

When DAM(a) 16 is detected at the aforementioned S3(a), the loop S4(a) is used to monitor with the timer 20 the time from the detection of the ID area 3 to the detection of DAM(a) 16.

[0026]

Next explained will be the timeout process for the Y case at S4(a), where the time from the detection of the ID area 3 to the detection of the DAM(a) 16 exceeds a given time period. If DAM(a) 16 is not detected even after the time from the detection of the ID area 3 to the detection of DAM(a) 16 exceeds the amounts of sync(a) 15 and DAM(a) 16 (i.e., after the passage of 16 bytes), at S3(b) DAM(b) 18 is detected and the frame synchronization signal c is output to the delay circuit 19.

[0027]

At the delay circuit 19, the frame synchronization signal c' is output without delaying the frame synchronization signal c. That is, synchronization is established by sync(a) 15, and at S5(b) DAM(a) 16 and sync(b) 17 are skipped and DAM(b) 18 is detected.

[0028]

The two causes of the non-detection of DAM(a) 16 are, first, a defective DAM(a) 16 itself and, second, the inability to detect the reproduction block signal because it was not generated by sync(a) 15. In the former case, the data area reproduced data e for detecting DAM(b) 18 by means of the aforementioned procedure is output; however, in the latter case, DAM(b) 18 also is undetectable by means of the aforementioned procedure. In this case, it is possible to detect DAM(b) 18 by means of the retry routine at S7. Next, this retry routine procedure will be explained with reference to Figure 4.

[0029]

That is, Figure 4 is a flowchart showing the retry routine. S8 indicates an ID detection means identical to [that of] S2. At S8, when the desired ID area 3 is detected, the clock synchronization circuit 10 is operated after a delay in the amount of sync(a) 15 and DAM(a) 16 (i.e., 16 bytes).

[0030]

Next, at the clock synchronization circuit 10, sync(b) 17 is used to generate the playback clock signal, the AM detection circuit 11 detects DAM(b) 18, and the frame synchronization signal c is output as the result of this detection. The frame synchronization signal c is input into the delay circuit 19 (S9). Here, however, the frame

synchronization signal c' is output without a delay (S10). The frame synchronization signal c' is input into the demodulation circuit 12, DAM(b) is output (S11), and the reproduced data e of data area 7 is output (S13). Also, at S11, if DAM(b) is not detected, a timeout (S12) results, so reproduction becomes impossible (S14).

[0031]

Consequently, according to the present embodiment, by alternately disposing multiple data area demodulation start position signals and synchronization signals, and by disposing the data area demodulation start position signal or multiple [copies] thereof, even if a bad sector results from a burst error of synchronization signal sync(a) or data area demodulation start position signal (DAM)(a), either of the data area demodulation start positions signals DAM(b) located thereafter may be detected, thereby dramatically improving the incidence of bad sectors attributable to error, in data portion 8.

[0032]

The sector format in the second embodiment of the present invention is shown in Figure 5. In the second embodiment, error-correction parity bytes 35 are added to the data portion of the first embodiment, and this is an error-correction code called interleaved Reed-Solomon.

[0033]

Figure 6 is a diagram showing the format of the error-correction code in Figure 5. The performance of the error-correction code of Figure 6 enables triple error [correction] of random errors. Also, for burst errors, it is possible to correct up to 11 continuous bytes of errors. Consequently, for the data area and error-correction parity bytes 35, it is possible to output the correct data area reproduced data e by means of the error-correction function, for burst errors up to 11 bytes.

[0034]

Figure 7 is the block diagram showing the configuration of the FD device of the second embodiment of the present invention. 36 is the error-correction circuit, and other symbols not explained hereinafter indicate functionalities identical or equivalent to those of symbols in previous diagrams.

[0035]

Regarding the operation of the second embodiment of the present invention, when an error occurs in the data area reproduced data e reproduced by means of the procedure in the first embodiment of the present invention, error-correction processing is performed by the error-correction circuit 36, and [the result] is output as the data area reproduced data e' .

[0036]

In addition, even if a burst error up to 11 bytes long occurs in the area in which sync and DAM are recorded, only one of the multiple recorded syncs [or] DAMs will become an error. Consequently, according to this second embodiment, even if a burst error up to 11 bytes is present anywhere in data portion 9, the correct data area reproduced data e' will be output.

[0037]

Here, supposing that the same error-correction parity bytes 35 as [those] in the second embodiment are added to the conventional sector format, when a burst error occurs in the data area 7 and the error-correction parity bytes 35, the correct data area reproduced data e can be output. However, when a burst error occurs elsewhere than in data area 7 [or] the error-correction parity bytes 35 (i.e., when a burst error occurs in sync 5 or DAM 6), DAM 6 cannot be detected, so the demodulation circuit 12 cannot operate and the center data cannot be reproduced.

[0038]

Consequently, when an error is caused by a burst error in the data portion 9, if a sync 5 and DAM 6 burst error occurs in the conventional sector format, the data cannot be reproduced, and it is highly probable that a bad sector will result. In the aforementioned second embodiment, however, the incidence of bad sectors resulting from sync and DAM burst errors is improved considerably.

[0039]

Thus, the aforementioned second embodiment has [the following] effects: It is only necessary to detect either the first sync(a) 15 [or] the second sync(b) 17 as well as either DAM(a) 16 [or] DAM(b) 18 located thereafter, so there is considerable improvement in the incidence of bad sectors attributable to the inability to generate the clock signal for reproduction and the inability to detect DAM, and the burst error-correction capability of the error-correction circuit 18 can be utilized well.

[0040]

[Effects of the Invention]

The floppy disk device of the present invention, which was explained previously, is equipped with multiple, alternate sync and DAM in the sector format, and [it] can considerably reduce the incidence of bad sectors attributable to the inability to detect DAM, because it is possible to reproduce the data area by generating a reproduction clock signal by means of either sync and detecting either DAM located thereafter.

[0041]

In addition, when an error-correction code is added to the data area to reduce the incidence of bad sectors attributable to bad sectors, each DAM is disposed at least the correctable burst error length apart, and sync is recorded thereafter. As a result, it is possible to significantly reduce the incidence of bad sectors attributable to DAM detection mistakes and reproduction clock signal generation trouble. Therefore, it is possible to make good use of the burst error-correction capability of the error-correction circuit.

[Brief Explanation of the Drawings]

[Figure 1]

A diagram showing the sector format in the first embodiment of the present invention.

[Figure 2]

A block diagram showing the configuration of the FD device in the first embodiment of the present invention.

[Figure 3]

A flowchart showing the configuration of the FD device of Figure 2.

[Figure 4]

The retry routine flowchart that explains the operation of the FD device of Figure 2.

[Figure 5]

A diagram showing the sector format in the second embodiment of the present invention.

[Figure 6]

A diagram showing the error-correction code format in Figure 5.

[Figure 7]

A block diagram showing the configuration of the FD device in the second embodiment of the present invention.

[Figure 8]

A diagram showing the sector format of a conventional FD device.

[Figure 9]

A block diagram showing the configuration of a conventional FD device.

[Explanation of the Symbols]

- 1 ID area synchronization signal (IDsync)
- 2 ID area demodulation start position signal (IDAM)
- 3 ID area
- 4 GAP2
- 7 Data area
- 8 ID portion
- 9 Data portion
- 10 Clock synchronization circuit
- 11 Demodulation start position signal detection circuit (AM detection circuit)
- 12 Demodulation circuit
- 14 CPU
- 15 1st data area synchronization signal (sync(a))
- 16 1st data area demodulation start position signal (DAM(a))
- 17 2nd data area synchronization signal (sync(b))
- 18 2nd data area demodulation start position signal (DAM(b))
- 19 Delay circuit
- 20 Timer
- 35 Error-correction parity bytes
- 36 Error-correction circuit

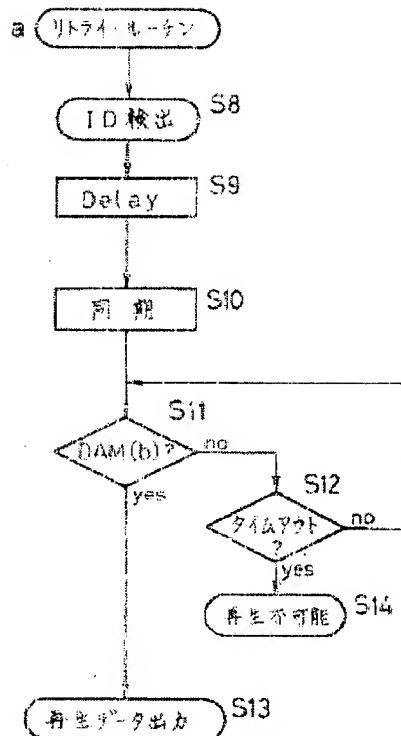


Figure 4

Key
 a Retry routine
 S8 ID detection
 S10 Synchronization
 S12 Timeout?
 S13 Reproduced data output
 S14 Reproduction impossible

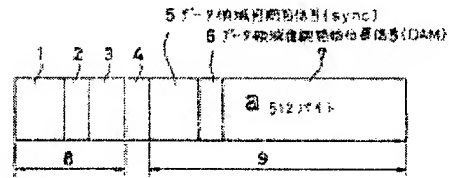


Figure 8

Key
 5 Data area synchronization signal (sync)
 6 Data area demodulation start position signal (DAM)
 a 512 bytes

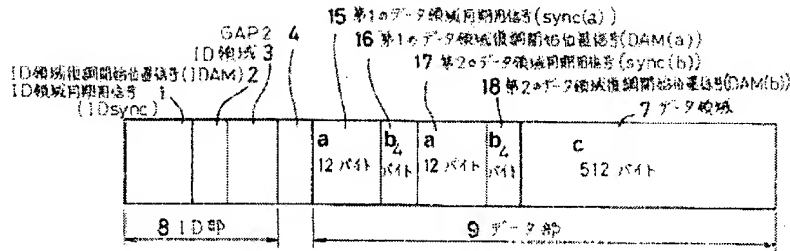


Figure 1

Key

- 1 ID area synchronization signal (IDsync)
- 2 ID area demodulation start position signal (IDAM)
- 3 ID area
- 7 Data area
- 8 ID portion
- 9 Data portion
- 15 1st data area synchronization signal (sync(a))
- 16 1st data area demodulation start position signal (DAM(a))
- 17 2nd data area synchronization signal (sync(b))
- 18 2nd data area demodulation start position signal (DAM(b))
- a 12 bytes
- b 4 bytes
- c 512 bytes

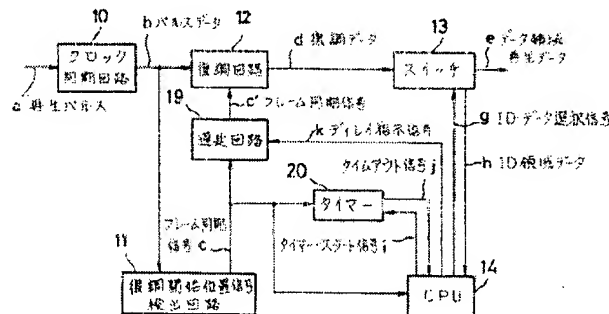


Figure 2

Key

- 10 Clock sync circuit
- 11 Demodulation start position signal detection circuit
- 12 Demodulation circuit
- 13 Switch
- 19 Delay circuit
- 20 Timer
- a Reproduction pulse
- b Pulse data
- c Frame synchronization signal
- c' Frame synchronization signal
- d Demodulated data
- e Data area reproduced data
- g ID-data select signal
- h ID area data
- i Timer start signal
- j Timeout signal
- k Delay indication signal

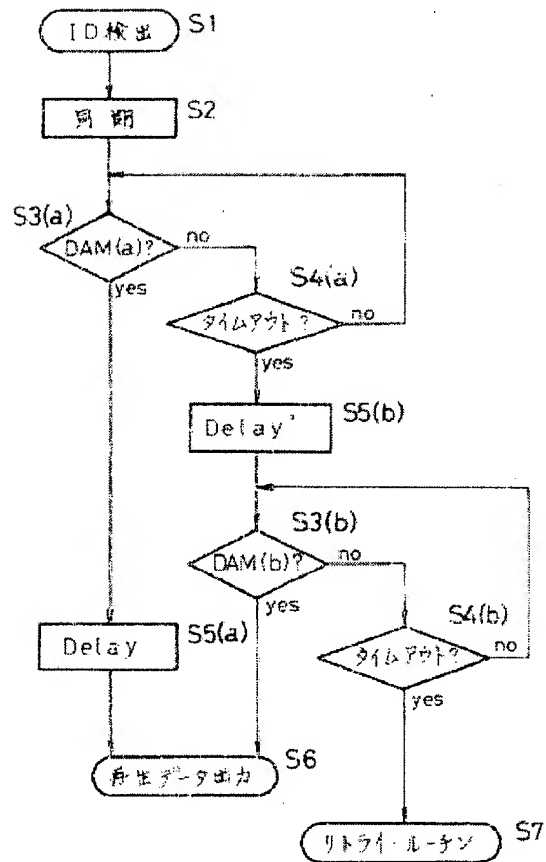


Figure 3

Key

- S1 ID detection
- S2 Synchronization
- S4(a) Timeout?
- S4(b) Timeout?
- S6 Reproduced data output
- S7 Retry routine

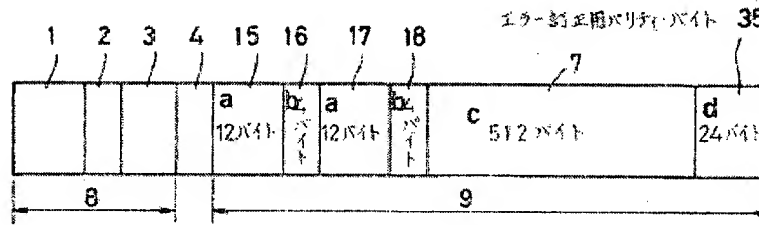


Figure 5

Key
 7 512 bytes
 a 12 bytes
 b 4 bytes
 c 512 bytes
 d 24 bytes

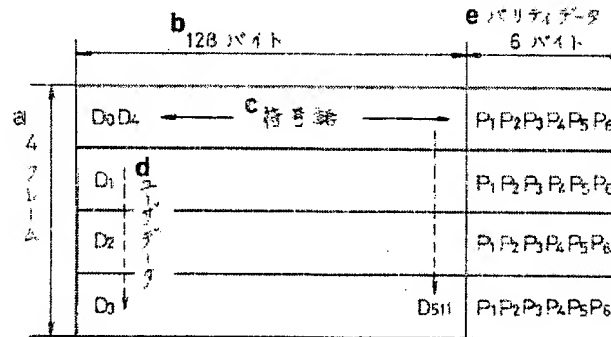


Figure 6

Key
 a 4 frames
 b 128 bytes
 c Code words
 d User data
 e Parity data, 6 bytes

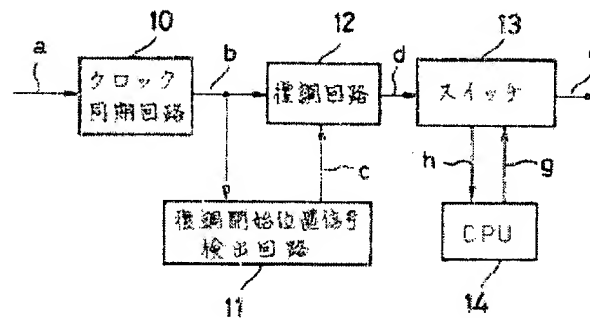


Figure 9

Key
 10 Clock sync circuit
 11 Demodulation start position signal detection circuit
 12 Demodulation circuit
 13 Switch

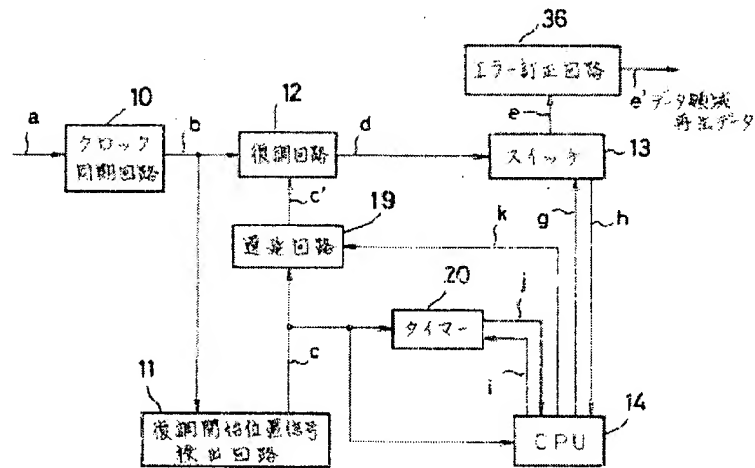


Figure 7

Key

- 10 Clock sync circuit
- 11 Demodulation start position signal detection circuit
- 12 Demodulation circuit
- 13 Switch
- 19 Delay circuit
- 20 Timer
- 36 Error-correction circuit
- e' Data area reproduced data